In the Claims

Claim 1 (original): A device associated with a semiconductor substrate and comprising:

an electrical node supported by the semiconductor substrate and comprising conductively-doped semiconductive material;

a first dielectric material comprising aluminum oxide;

a second dielectric material comprising a metal oxide selected from the group consisting of hafnium oxide, tantalum oxide, titanium oxide and zirconium oxide; and

wherein the first dielectric material is between the second dielectric material and the conductively-doped semiconductive material.

Claim 2 (original): The device of claim 1 wherein the conductively-doped semiconductive material comprises conductively-doped silicon.

Claim 3 (original): The device of claim 1 wherein the conductively-doped semiconductive material consists essentially of conductively-doped silicon.

Claim 4 (original): The device of claim 1 wherein the conductively-doped semiconductive material consists of conductively-doped silicon.

Claim 5 (original): The device of claim 1 wherein the second dielectric material consists essentially of hafnium oxide.

Claim 6 (original): The device of claim 1 wherein the second dielectric material consists of hafnium oxide.

Claim 7 (original): The device of claim 1 wherein the second dielectric material consists essentially of tantalum oxide.

Claim 8 (original): The device of claim 1 wherein the second dielectric material consists of tantalum oxide.

Claim 9 (original): The device of claim 1 wherein the second dielectric material consists essentially of zirconium oxide.

Claim 10 (original): The device of claim 1 wherein the second dielectric material consists of zirconium oxide.

Claim 11 (original): The device of claim 1 wherein the first dielectric material consists essentially of aluminum oxide.

Claim 12 (original): The device of claim 1 wherein the first dielectric material consists of aluminum oxide.

Claim 13 (original): The device of claim 12 wherein the first dielectric material has a pair of opposing surfaces with one of the opposing surfaces being in physical contact with the conductively-doped silicon and the other of the opposing surfaces being in physical contact with the metal oxide of the second dielectric material.

Claim 14 (original): The device of claim 13 wherein the first dielectric material has a thickness between the opposing surfaces of from about 5Å to about 60Å.

Claim 15 (original): The device of claim 13 wherein the second dielectric material consists of the metal oxide and has a thickness of from about 20Å to about 90Å.

Claim 16 (original): The device of claim 1 comprising a capacitor electrode over the second dielectric material and being a capacitor.

Claim 17 (original): A DRAM array comprising one or more of the capacitor constructions of claim 16.

Claim 18 (original): An electronic system comprising the DRAM array of claim 17.

Claim 19 (original): A capacitor construction comprising:

a first capacitor electrode comprising conductively-doped silicon;

a second capacitor electrode comprising one or more materials selected from the group consisting of metals and metal compounds;

a first dielectric layer between the first and second capacitor electrodes, the first dielectric layer comprising aluminum oxide;

a second dielectric layer between the first and second capacitor electrodes, the second dielectric layer comprising a metal oxide other than aluminum oxide;

wherein the first dielectric layer is between the second dielectric layer and the conductively-doped silicon; and

wherein the metal oxide of the second dielectric layer is in physical contact with the second capacitor electrode.

Claim 20 (original): The capacitor construction of claim 19 further comprising one or more additional dielectric layers between the first and second capacitor electrodes besides the first and second dielectric layers.

Claim 21 (original): The capacitor construction of claim 19 wherein the first and second dielectric layers are the only dielectric layers between the first and second capacitor electrodes.

Claim 22 (original): The capacitor construction of claim 21 wherein the first and second dielectric layers have a combined thickness of from about 25Å to about 150Å.

Claim 23 (original): The capacitor construction of claim 22 wherein the first dielectric layer has a thickness of from about 5Å to about 60Å.

Claim 24 (original): The capacitor construction of claim 22 wherein the second dielectric layer has a thickness of from about 20Å to about 90Å.

Claim 25 (original): The capacitor construction of claim 21 wherein the first and second dielectric layers have a combined thickness of from about 25Å to about 80Å.

Claim 26 (original): The capacitor construction of claim 25 wherein the first dielectric layer has a thickness of from about 5Å to about 20Å.

Claim 27 (original): The capacitor construction of claim 25 wherein the second dielectric layer has a thickness of from about 20Å to about 60Å.

Claim 28 (original): The capacitor construction of claim 19 wherein the metal oxide of the second dielectric layer is selected from the group consisting of hafnium oxide, tantalum oxide and zirconium oxide.

Claim 29 (original): The capacitor construction of claim 28 wherein the second dielectric layer consists essentially of hafnium oxide.

Claim 30 (original): The capacitor construction of claim 28 wherein the second dielectric layer consists of hafnium oxide.

Claim 31 (original): The capacitor construction of claim 28 wherein the second dielectric layer consists essentially of tantalum oxide.

Claim 32 (original): The capacitor construction of claim 28 wherein the second dielectric layer consists of tantalum oxide.

Claim 33 (original): The capacitor construction of claim 28 wherein the second dielectric layer consists essentially of zirconium oxide.

Claim 34 (original): The capacitor construction of claim 28 wherein the second dielectric layer consists of zirconium oxide.

Claim 35 (original): The capacitor construction of claim 19 wherein the aluminum oxide of the first dielectric layer is physically against the conductively-doped silicon of the first capacitor electrode.

Claim 36 (original): The capacitor construction of claim 19 wherein:

the first dielectric layer consists of aluminum oxide;

the first dielectric layer has a pair of opposing surfaces;

one of the opposing surfaces of the first dielectric layer is physically against the conductively-doped silicon of the first capacitor electrode; and

the other of the opposing surfaces of the first dielectric layer is physically against the metal oxide of the second dielectric layer.

Claim 37 (original): The capacitor construction of claim 36 wherein the first dielectric layer has a thickness between the opposing surfaces of from about 5Å to about 20Å.

Claim 38 (original): The capacitor construction of claim 36 wherein the second dielectric layer consists of hafnium oxide.

Claim 39 (original): The capacitor construction of claim 36 wherein the second dielectric layer consists of tantalum oxide.

Claim 40 (original): The capacitor construction of claim 36 wherein the second dielectric layer consists of zirconium oxide.

Claim 41 (currently amended): A DRAM array comprising: ~~one or more of the capacitor constructions of claim 19~~

a plurality of wordlines;

a plurality of bitlines; and

a plurality of capacitor constructions electrically accessible through the wordlines and bitlines, at least one of the capacitor constructions including:

a first capacitor electrode comprising conductively-doped silicon;

a second capacitor electrode comprising one or more materials selected from the group consisting of metals and metal compounds;

a first dielectric layer between the first and second capacitor electrodes, the first dielectric layer comprising aluminum oxide;

a second dielectric layer between the first and second capacitor electrodes, the second dielectric layer comprising a metal oxide other than aluminum oxide;

wherein the first dielectric layer is between the second dielectric layer and the conductively-doped silicon; and

wherein the metal oxide of the second dielectric layer is in physical contact with the second capacitor electrode.

Claim 42 (currently amended): An electronic system comprising: ~~the DRAM array of claim 41~~

a memory device; and

a processor in electrical communication with the memory device; and

wherein at least one of the memory device and the processor includes a memory cell comprising a capacitor construction which includes:

a first capacitor electrode comprising conductively-doped silicon;

a second capacitor electrode comprising one or more materials selected from the group consisting of metals and metal compounds;

a first dielectric layer between the first and second capacitor electrodes, the first dielectric layer comprising aluminum oxide;

a second dielectric layer between the first and second capacitor electrodes, the second dielectric layer comprising a metal oxide other than aluminum oxide;

wherein the first dielectric layer is between the second dielectric layer and the conductively-doped silicon; and

wherein the metal oxide of the second dielectric layer is in physical contact with the second capacitor electrode.

Claims 43-62 (canceled).